



ANALYSIS AND DESIGN OF DOUBLE TAIL DYNAMIC COMPARATOR IN ANALOG TO DIGITAL CONVERTER

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Abstract: The need for ultra low-power, area efficient and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. The objective of this paper is to design and implementation of delay efficient and low power consumption double-tail dynamic comparator in successive approximation analog to digital convertor. The conventional double tail comparator is modified for low-power and fast operation even in small supply voltages. But the double tail comparator both power consumption and delay will be reduced.

Keywords-Double-tail dynamic comparator, high-speed analog-to-digital converters (ADCs), Successive Approximation ADC.

I. INTRODUCTION

Comparator is one of the fundamental building blocks in most analog-to-digital converters (ADCs). Many high speed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area. Some ADC architectures use a positive feedback which results in the voltage variations disturbing the input voltage which is kickback noise. In this paper, a comprehensive analysis about the delay of dynamic comparators has been presented for various architectures. Furthermore, based on the double-tail structure in a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay

time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double-tail comparator.

II. CLOCKED REGENERATIVE COMPARATORS

Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. Recently, many comprehensive analyses have been presented, which investigate the performance of these comparators from different aspects, such as noise offset, and random decision errors, and kick-back noise In this section, a comprehensive delay analysis is presented; the delay time of two common

structures, i.e., conventional dynamic comparator and conventional double-tail comparator is analyzed, based on which the high speed double tail dynamic comparator will be presented.

A. Conventional Dynamic Comparator

The conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power Consumption. The operation of the comparator is during the reset phase when $CLK = 0$ and M_{tail} is off, reset transistors ($M7-M8$) pull both output nodes $Outn$ and $Outp$ to VDD to define a start condition and to have a valid logical level during reset. In the comparison phase, when $CLK = VDD$, transistors $M7$ and $M8$ are off, and M_{tail} is on. Output voltages ($Outp$, $Outn$), which had been pre-charged to VDD , start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where $V_{INP} > V_{INN}$, $Outp$ discharges faster than $Outn$, hence when $Outp$, falls down to $VDD - |V_{thp}|$ before $Outn$ (discharged by transistor $M1$ drain current), the corresponding PMOS transistor ($M5$) will turn on initiating the latch regeneration caused by back-to-back inverters ($M3, M5$) and ($M4, M6$). $Outn$ pulls to VDD and $Outp$ discharges to ground. The disadvantage of this comparator is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. Also that it consists of only one tail which is the current path M_{tail} , which defines the current for both differential amplifier and the latch.

B. Conventional Double-Tail Dynamic Comparator

A conventional double-tail comparator has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables

both a large current in the latching stage and wider M_{tail2} , for fast latching independent of the input common-mode voltage (V_{cm}), and a small current in the input stage (small M_{tail1}). During reset phase ($CLK = 0$, M_{tail1} , and M_{tail2} are off), transistors $M3-M4$ pre-charge fn and fp nodes to VDD , which in turn causes transistors $MR1$ and $MR2$ to discharge the output nodes to ground. During decision-making phase ($CLK = VDD$, M_{tail1} and M_{tail2} turn on), $M3-M4$ turn off and voltages at nodes fn and fp start to drop with the rate defined by $I_{M_{tail1}}/C_{fn(p)}$ and on top of this, an input-dependent differential voltage $_V_{fn(p)}$ will build up. The intermediate stage formed by $MR1$ and $MR2$ passes $_V_{fn(p)}$ to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise.

III. HIGH SPEED DOUBLE-TAIL DYNAMIC COMPARATOR

The high speed dynamic double-tail comparator due to the better performance of double-tail architecture in low-voltage applications, the comparator is designed based on the double-tail structure. The main idea of this comparator is to increase $_V_{fn/fp}$ in order to increase the latch regeneration speed. For this purpose, two control transistors ($Mc1$ and $Mc2$) have been added to the first stage in parallel to $M3/M4$ transistors but in a cross coupled manner.

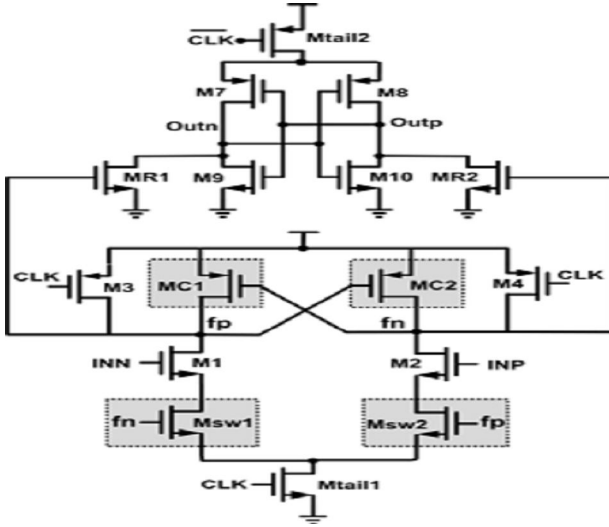


Fig1. Double tail dynamic comparator

A. Delay Analysis

However; the dynamic comparator enhances the speed of the double-tail comparator by affecting two important factors: first, it increases the initial output voltage difference (V_0) at the beginning of the regeneration ($t = t_0$); and second, it enhances the effective transconductance (g_{meff}) of the latch.

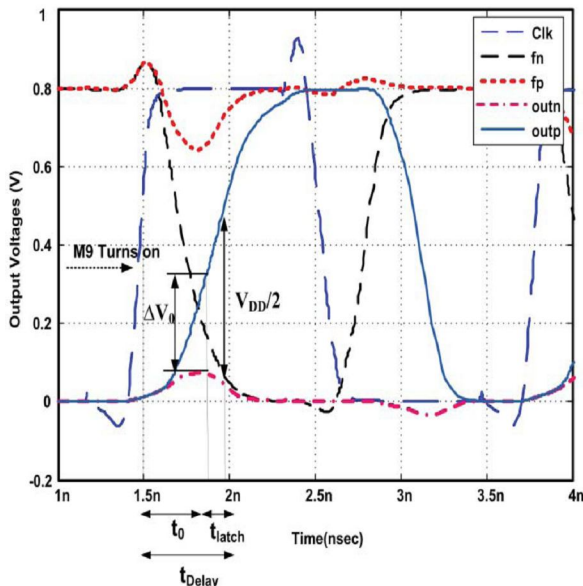


Fig2. Transient simulations of the double-tail dynamic comparator for input voltage difference of $V_{\text{in}} = 5 \text{ mV}$, $V_{\text{cm}} = 0.7 \text{ V}$, and $V_{\text{DD}} = 0.8 \text{ V}$.

1) Reducing the Energy per Comparison:

It is not only the delay parameter which is improved in the modified double tail dynamic comparator, but the energy per conversion is reduced as well. In conventional double-tail topology, both fn and fp nodes discharge to the ground during the decision making phase and each time during the reset phase they should be pulled up back to the VDD. However, in double-tail dynamic comparator, only one of the mentioned nodes (fn/fp) has to be charged during the reset phase. This is due to the fact that during the previous decision making phase, based on the status of control transistors, one of the nodes had not been discharged and thus less power is required.

B. Kickback Noise

Principally in latched comparators, the large voltage variations on the regeneration nodes are coupled, through the parasitic capacitances of the transistors, to the input of the comparator. Since the circuit preceding it does not have zero output impedance, the input voltage is disturbed, which may degrade the accuracy of the converter. This disturbance is usually called "kickback noise".

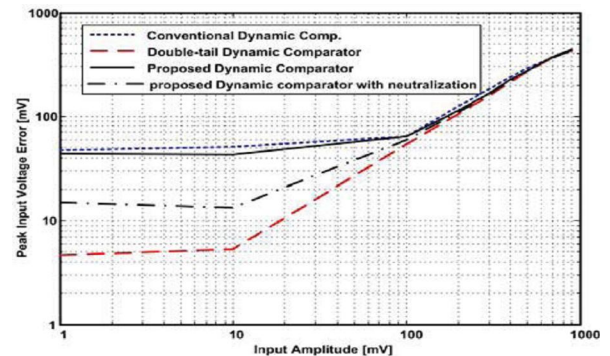


Fig3. Peak input voltage error due to Kickback Noise

TABLE- 1
PERFORMANCE COMPARISON

Comparat or structure	Convention al dynamic comparator	Double tail dynamic comparat or	High speed Double tail dynamic comparat or
Technolog y CMOS	180nm	180nm	180nm
Supply voltage	0.8v	0.8v	0.8v
Sampling frequency	900MHZ	1.8GHZ	2.4GHZ
Delay	940	358	294
Kickback noise voltage	51.3mv	53mv	43mv
Input offset voltage	7.89mv	7.91mv	7.8mv
Estimated area	16 μ x16 μ	28 μ x12 μ	28 μ x14 μ

IV PROPOSED SYSTEM

A) Analog To Digital Converter

An **analog-to-digital converter** is a device that converts a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude. ADC may also provide an isolated measurement such as an electronic device that converts an input analog voltage or current to a digital number proportional to the magnitude of the voltage or current. However, some non-electronic or only partially electronic devices, such as rotary encoders, can also be considered ADCs. The

digital output may use different coding schemes. Typically the digital output will be a two's complement binary number that is proportional to the input, but there are other possibilities. An encoder, for example, might output a Gray code.

The inverse operation is performed by a digital-to-analog converter (DAC)

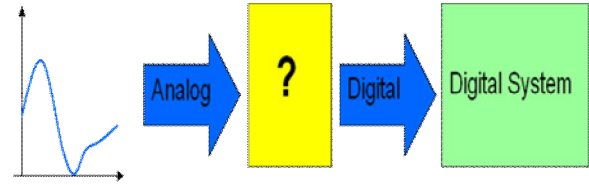


Fig4 analog to digital converter

B) TYPES OF ADC AND COMPARISON

- Flash ADC
- Sigma-delta ADC
- Dual slope converter
- Successive approximation converter

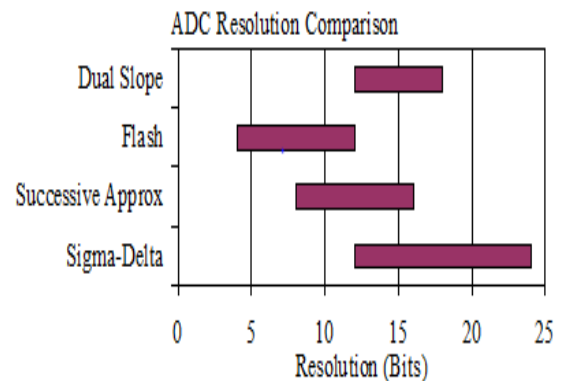


TABLE 2
ADC COMPARISON

Type	Speed (relative)	Cost (relative)
Dual Slope	Slow	Med
Flash	Very Fast	High
Successive Approx	Medium – Fast	Low
Sigma-Delta	Slow	Low

V. SUCCESSIVE APPROXIMATION REGISTER

Successive-approximation-register (SAR) analog-to-digital converters (ADCs) represent the majority of the ADC market for medium- to high-resolution ADCs. SAR ADCs provide up to 5MSPS sampling rates with resolutions from 8 to 18 bits. The SAR architecture allows for high-performance, low-power ADCs to be packaged in small form factors for today's demanding applications. The basic principle of this A/D converter is that the unknown analog input voltage is approximated against an n-bit digital value trying one bit at a time, beginning with the MSB. This type of A/D converter operates by successively dividing the voltage range by half, as explained in the following

Steps:

- The MSB is initially set to 1 with the remaining three bits 0. The digital equivalent is compared with the unknown analog input voltage.
- If the input voltage is higher than the digital equivalent, the MSB is retained as 1 and the second MSB is set to 1. Otherwise, the MSB is set to 0 and the second MSB is set to 1.

We are replaced in this comparator by using successive approximation ADC.

The R-2R resistor ladder network directly converts a parallel digital symbol/word into an analog voltage. Each digital input (b0, b1, etc.)

adds its own weighted contribution to the analog output. In digital circuits, a **shift register** is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the "bit array" stored in it, shifting in the data present at its input and shifting out the last bit in the array, at each transition of the clock input.

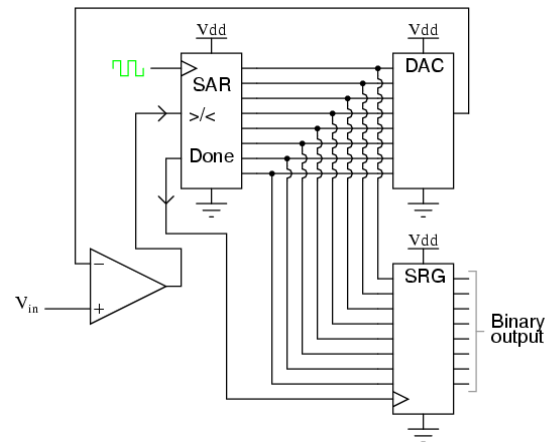
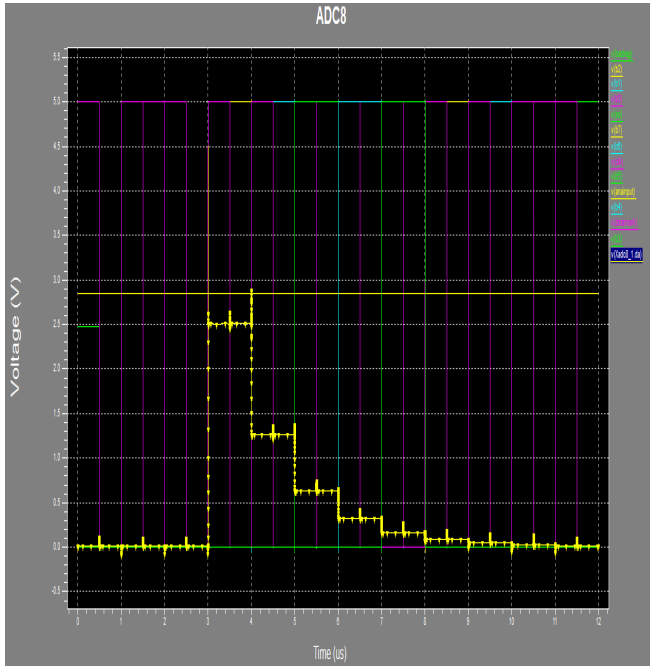


Fig5. Successive Approximation Register

VI SIMULATION RESULT

As Successive Approximation Register is the slowest ADC we implement the high speed double tail comparator in the Successive Approximation Register, and analyze the delay, speed and yield range of the analog to digital converter. The basic principle of this A/D converter is that the unknown analog input voltage is approximated against an n-bit digital value trying one bit at a time, beginning with the MSB.



VII CONCLUSION

We presented a comprehensive delay analysis for clocked dynamic comparators. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new high speed dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 0.18- μm CMOS technology confirmed that the delay and energy per conversion of the high speed dynamic comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator. And also implement the high speed double tail dynamic comparator in successive approximation ADC. So the main advantage is very low power consumption.

VII FUTURE SCOPE

The proposed comparator is operated with very less voltage ie. Is 0.8v. so it require very less power consumption for the operation and also it switches very faster than the existing comparators. Finally we were implemented the analog to digital converter using our proposed double tail comparator. It requires very less power consumption while comparing to the existing comparators. So in future we use this Analog to digital converter in the mobile phones, laptops and analog and mixed signal processing, etc.

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